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EXAMINER	
CHOU, ANDREW Y	

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,264	WOLCZKO ET AL.	
	Examiner	Art Unit	
	ANDREW CHOU	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response the amendment posted on 05/21/2008

2. Claims 18-19 are amended. Claims 1-22 are pending.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/21/2008 has been entered.

Response to Arguments

4. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection. See Talcott prior art made or record below.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 18-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter:

Claim 18 is non-statutory as being "a sampling mechanism for sampling an instruction executing in a multi-threaded processor comprising...sampling logic...sampling register logic...instruction history registry logic...sample filtering...", thus the sampling mechanism is not yet embodied in executable code format as a computer component. Thus, the computer program product is computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer- readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, it is important to distinguish claims that define descriptive material per se from claims that define statutory inventions. MPEP 2106.01 (I).

Claims 19-22 are also non-statutory as being " a sampling mechanism" thus the sampling mechanism is not yet embodied in executable code format as a computer component. Thus, the computer program product is computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Talcott et al. US 7,096,390 B2 (hereinafter Talcott).

Claim 1:

Talcott discloses a method of sampling instructions executing in a multi-threaded processor comprising:

selecting an instruction for sampling (see for example col. 2: 59-66, "If a sampled instruction meets certain criteria, the instruction becomes a reporting candidate.");

storing sampling information relating to the instruction (see for example col. 2:66-68, "…instruction history…");

determining whether the sampling information includes an event of interest, the event of interest to a particular thread, within which the instruction is executing (see for example Figure 1, item 102, "sampling mechanism", and related text);

and reporting the sampling information to the particular thread when the sampling information includes an event of interest on a per-thread basis (see for example Figure 2A, step 240, "Did selected instruction match the filtering criteria", and related text).

Claim 2:

Talcott further discloses the method of claim 1 further comprising providing a register with a bit vector representing a plurality of events of interest (see for example col. 2:65-col. 3:5); and

wherein the determining whether the sampling information includes the event of interest further includes comparing the sampling information relating to the instruction to the bit vector (see for example col. 2:65- col. 3:5).

Claim 3:

Talcott further discloses the method of claim 2 wherein the comparing is via at least one of a mask operation or a more expressive operation (see for example Figure 2A, step 240, and related text)).

Claim 4:

Talcott further discloses the method of claim 1 wherein the selecting the instruction is without regard to a thread to which the instruction is bound (see for example Figure 2A, step 222, and related text).

Claim 5:

Talcott further discloses the method of claim 1 further comprising identifying a thread to which the instruction is bound when the instruction is selected (see for example col. 5:1-21).

Claim 6:

Talcott further discloses the method of claim 1 further comprising providing filtering criteria on a per-thread basis (see for example col. 5:1-21).

Claim 7:

Talcott further discloses the method of claim 1 further comprising providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see for example Figure 2A, step 210, "Software sets filtering criteria and loads candidate counter register with non-zero values, which starts sampling logic", and related text).

Claim 8:

Talcott discloses a method of sampling instructions executing in a multi-threaded processor comprising: setting a candidate counter to a number (see for example Figure 2A, step 210, and related text);

selecting an instruction for sampling (see for example Figure 2A, step 226, "...selects...instruction...", and related text);

storing information relating to the instruction (see for example Figure 2A, step 230, and related text);

determining whether all events for the instruction have occurred (see for example Figure 2A, step 236, "Have all possible events for the selected instruction occured?", and related text);

decrementing the candidate counter when all events for the instruction have occurred and when the instruction corresponds to a desired sampled thread (see for example col. 3:64-col. 4:5);

determining whether the candidate counter equals zero (see for example col. 4:1-16); and reporting the instruction when the candidate counter equals zero (see for example col. 4:1-16).

Claim 9:

Talcott further discloses the method of claim 8 wherein the information relating to the instruction represents an instruction history (see for example Figure 1, item 122, "instruction history registers", and related text), and the instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privilege value, a branch history value and a number in fetch bundle value (see for example Figure 1, item 122, and related text).

Claim 10:

Talcott further discloses the method of claim 8 wherein the selecting the instruction is without regard to a thread to which the instruction is bound(see for example Figure 2A, step 222, and related text).

Claim 11:

Talcott further discloses the method of claim 8 further comprising identifying a thread to which the instruction is bound when the instruction is selected (see for example col. 5:1-21).

Claim 12:

Talcott further discloses the method of claim 8 further comprising providing filtering criteria on a per-thread basis (see for example col. 5:1-21).

Claim 13:

Talcott further discloses the method of claim 8 further comprising providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see for example Figure 2A, step 210, "Software sets filtering criteria and loads candidate counter register with non-zero values, which starts sampling logic", and related text).

Claim 14:

Talcott discloses a method of sampling instructions executing in a multi-threaded processor comprising:

setting a candidate counter to a number selecting an instruction for sampling (see for example Figure 2A, step 210, and related text);

storing information relating to the instruction (see for example Figure 2A, step 230, and related text);

determining whether all events for the instruction have occurred (see for example Figure 2A, step 236, "Have all possible events for the selected instruction occured?", and related text);

determining whether the instruction includes events of interest, the events of interest including whether the instruction corresponds to a desired sampled thread (see for example Figure 2A, step 236, and related text);

decrementing the candidate counter when all events for the instruction have occurred and when the instruction includes events of interest (see for example col. 3:64-col. 4:5);

determining whether the candidate counter equals zero (see for example col. 4:1-16); and

reporting the instruction when the candidate counter equals zero (see for example col. 4:1-16).

Claim 15:

Talcott further discloses the method of claim 14 further comprising providing a register with a bit vector representing events of interest; and wherein the determining whether the instruction includes events of interest further includes comparing the information relating to the instruction to the bit vector (see for example col. 3:5-21, "...bit vector...").

Claim 16:

Talcott further discloses the method of claim 14 wherein the information relating to the instruction represents an instruction history, and the instruction history includes information relating to at least one of an event value, a program counter value, a branch target address value, an

effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number

in fetch bundle value (see for example Figure 1, item 122, "instruction history registers", and related text).

Claim 17:

Talcott further discloses the method of claim 14 wherein the selecting an instruction for sampling is based upon sample selection criteria; and the sample selection criteria include information relating to a desired sampled thread (see for example col. 4:31-44).

Claim 18:

Talcott discloses a sampling mechanism for sampling an instruction executing in a multi-threaded processor comprising:

sampling logic, the sampling logic determining whether the instruction corresponds to a desired sampled thread (see for example Figure 1, item 120, "Sampling Logic", and related text);

sampling register logic coupled to the sampling logic (see for example Figure 1, item 124, "Sampling Registers", and related text);

instruction history register logic coupled to the sampling register logic, the instruction history register logic storing information relating to the instruction (see for example Figure 1, item 122, and related text);

sample filtering and counting logic coupled to the sampling logic (see for example Figure 1, item 126, and related text); and

wherein the sample filtering and counting logic is replicated on a per thread basis see for example Figure 2, step 240, and related text).

Claim 19:

Talcott further discloses the sampling mechanism of claim 18 further comprising: notification logic, the notification logic reporting the information relating to the instruction if the instruction corresponds to the desired sampled thread (see for example Figure 1, item 128, "Notification Logic", and related text).

Claim 20:

Talcott further discloses the sampling mechanism of claim 18 wherein the sampling register logic includes a register with a bit vector representing events of interest; and wherein the sampling logic determines whether the instruction includes events of interest by comparing the information relating to the instruction to the bit vector (see for example col. 2:65- col. 3:5).

Claim 21:

Talcott further discloses the sampling mechanism of claim 18 wherein the information relating to the instruction represents an instruction history (see for example Figure 1, item 122, "instruction history registers", and related text), and the instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number in fetch bundle value (see for example Figure 1, item 122, and related text).

Claim 22:

Talcott further discloses the sampling mechanism of claim 18 wherein the sampling register logic includes a sample selection criteria register storing sample selection

criteria (see for example Figure 1, item 122, and related text); and the sample selection criteria include information relating to a desired sampled thread (see for example col. 3:44-56).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Y. Chou whose telephone number is (571) 272-6829. The examiner can normally be reached on Monday-Friday, 8:00 am - 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached on (571) 272-3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair- direct.uspto.,qov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

/Andrew Chou/

Examiner, Art Unit 2192

/Tuan Q. Dam/

Supervisory Patent Examiner, Art Unit 2192